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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Applicant: Trelewicz	Art Unit: 2122
Serial No.: 09/693,090	Examiner: Kiss
Filed: October 20, 2000	BLD9-2000-0060-US2
For: **COMPILER FOR ENABLING MULTIPLE SIGNED INDEPENDENT DATA ELEMENTS PER REGISTER**	June 2, 2004 750 B STREET, Suite 3120 San Diego, CA 92101

RESPONSE TO OFFICE ACTION

Commissioner of Patents and Trademarks
Washington, DC 20231

Dear Sir:

In response to the Office Action dated March 25, 2004, please amend the above-captioned patent application as follows. Correct an informality on the top of page 4 and amend the claims as indicated.

1169-6.AMD

Accordingly, a general purpose computer includes a compiler receiving higher-level code and outputting lower-level code to enable a processor to simultaneously process multiple multi-bit data elements in a single register. The logic of the lower-level code that is output by the compiler includes establishing at least first and second signed, multi-bit data elements in at least a first register, and simultaneously processing the elements. The precision for these packed elements determines their packing configuration. In this disclosure, "input precision" is used to reference the initial precision of individual data elements ~~prior to~~ after simultaneous operation, while "output precision" is used to reference the final maximum precision of individual data elements prior to simultaneous operations have been completed.